

Chapter 41 Level Shifter

In this chapter, we will introduce the level shifter circuits. Throughout the whole chapter, the following assumptions are made.

- (1) There are two VDDs in our circuit. They are V_{DDH} and V_{DDL} .
- (2) The input is a sequence of pulses.

The level shifter circuit will either increase the height of the pulses from V_{DDL} to V_{DDH} or decrease the height of pulses from V_{DDH} to V_{DDL} . Thus, there are two kinds of level shifters: the increasing level shifter and the decreasing level shifter.

We further require that there will be no current flowing in the level shifters.

Section 41.1 An Increasing Level Shifter Circuit

Fig. 41.1-1 shows an increasing level shifter circuit. The analysis of this circuit is as follows:

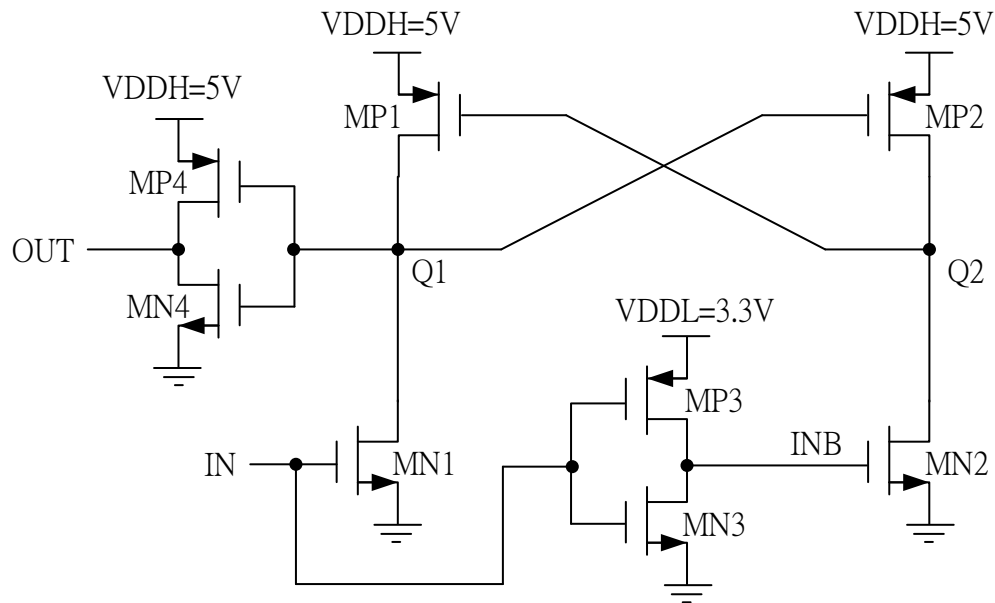


Fig. 41.1-1 An increasing level shifter

We assume that V_{in} is a sequence of pulses and its height is V_{DDL} which is 3.3V. We want to increase the height of the pulses from 3.3V to 5V

Case 1: V_{in} is 3.3V.

In this case, MN1 will be turned on and Q1 will be low. Note that MP2 will also be turned on because Q1 is low. MP4 and MN4 constitute an inverter. Thus, V_{out} will be high. Since MP4 is connected to V_{DDH} , the height of the output sequence will be 5 volts.

V_{in} is also sent to the inverter consisting of MP3 and MN3. INB will be therefore low and will turn off MN2. Since MP2 is turned on, Q2 will be high. Since Q2 is high, MP1 will be turned off.

In summary, when V_{in} is high, MN1 and MP2 will be turned on, MN2 and MP1 will be turned off, Q1 will be low, Q2 will be high and V_{out} will be high.

Case 2: V_{in} is 0V

In this case, MN1 will be turned off and MN2 will be turned on. Q2 will be low and will turn on MP1. Q1 will be high. Since Q1 is high, MP2 will be turned off and Vout will be low.

In summary, when Vin is 0V, MN2 and MP1 will be turned on, MN1 and MP2 will be turned off, Q1 will be high, Q2 will be 0V and Vout will be 0V.

The reader should note that no current will flow in the circuit.

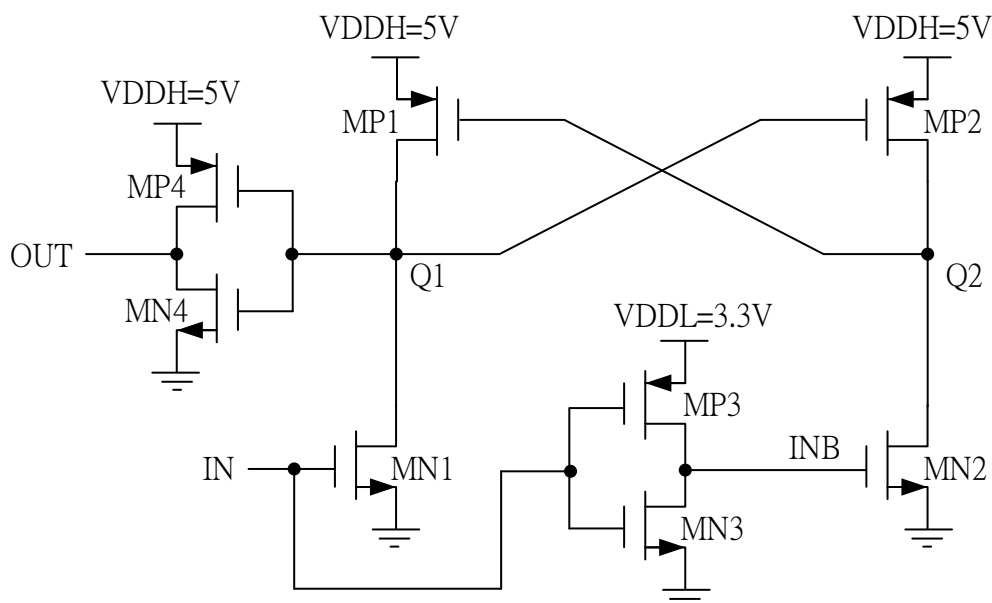


Fig. 41.1-1 The first level shifter circuit

Experiment 41.1-1 The Testing of the Increasing Level Shifter

In this experiment, the circuit is the one shown in Fig. 41.1-1. The program is in Table 41.1-1 and the results are in Fig. 41.1-2. We can see that the height of the sequence is lifted from 3.3v to 7v.

Table 41.1-1 The program of Experiment 41.1-1

```
Level Shifter
.PROTECT
.OPTION POST
.lib 'C:\model\tsmc\MIXED035\mm0355v.l' TT
.unprotect
.op
.options nomod post
```

```

VDDH VDDH 0 5V
VDDL VDDL 0 3.3V
VSS VSS 0 0V

MP1 Q1 Q2 VDDH VDDH PCH W=50U L=2U
MP2 Q2 Q1 VDDH VDDH PCH W=50U L=2U
MP3 INB IN VDDL VDDL PCH W=50U L=2U
MP4 OUT Q1 VDDH VDDH PCH W=50U L=2U
MN1 Q1 IN VSS VSS NCH W=50U L=2U
MN2 Q2 INB VSS VSS NCH W=50U L=2U
MN3 INBIN VSS VSS NCH W=50U L=2U
MN4 OUT Q1 VSS VSS NCH W=50U L=2U

VIN IN 0 pulse(0v 3.3v 20us 0.01us 0.01us 20us 40us)

.tran 1us 200us
.end

```

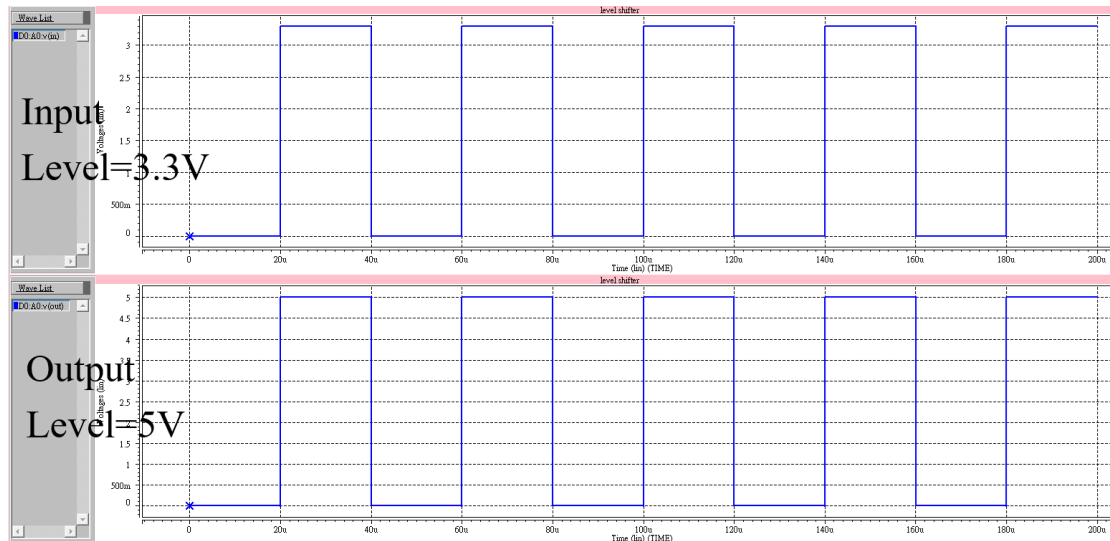


Fig. 41.1-2 The result of Experiment 41.1-1

Section 41.2 A Decreasing Level Shifter from 5V to 3.3V

Fig. 41.2-1 shows a decreasing level shifter circuit.

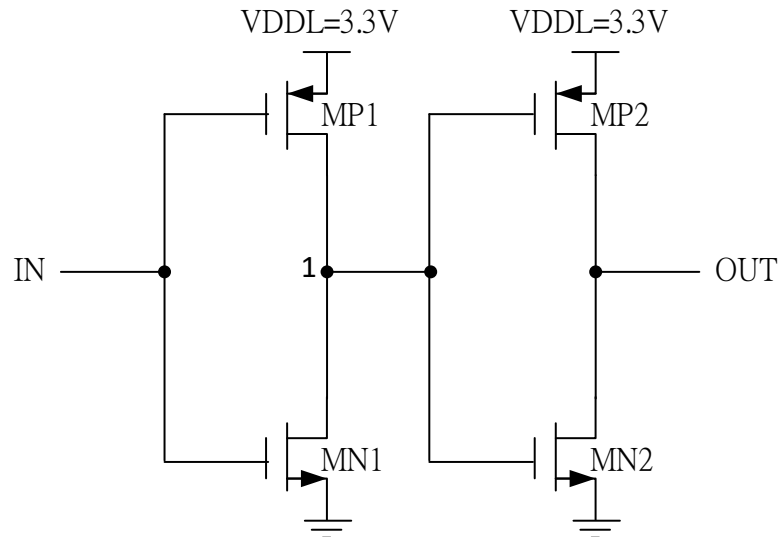


Fig.41.2-1 A Decreasing level shifter

It can be seen that this circuit consists of two inverters. Assume that the height of the input pulses is 5V. Since MP2 is connected to 3.3V, the height of the output pulses will be 3.3V. Thus, this circuit is a decreasing level shifter.

The reader may wonder whether this circuit can be used as an increasing level shifter. It cannot be because if the height of the input pulses is lower than 3.3V, PM1 and MN1 will both be turned on and current will flow. This violates our requirement specified at the beginning of this chapter.

Experiment 41.2-1 The Testing of the Decreasing Level Shifter

In this experiment, the circuit is in Fig. 41.2-1, the program is in Table 41.2-1 and the result is in Fig. 41.2-2.

Table 41.2-1 The program of Experiment 41.1-2

Level Shifter .PROTECT .OPTION POST .lib 'C:\model\tsmc\MIXED035\mm0355v.l' TT .unprotect

```

.op
.options nomod post

VDDH VDDH 0 5V
VDDL VDDL 0 3.3V
VSS VSS 0 0V

MP1 1 IN VDDL VDDH PCH W=50U L=2U
MP2 OUT 1 VDDL VDDH PCH W=50U L=2U
MN1 1 IN VSS VSS NCH W=50U L=2U
MN2 OUT 1 VSS VSS NCH W=50U L=2U

VIN IN 0 pulse(0v 5v 20us 0.01us 0.01us 20us 40us)

.tran 1us 200us
.end

```

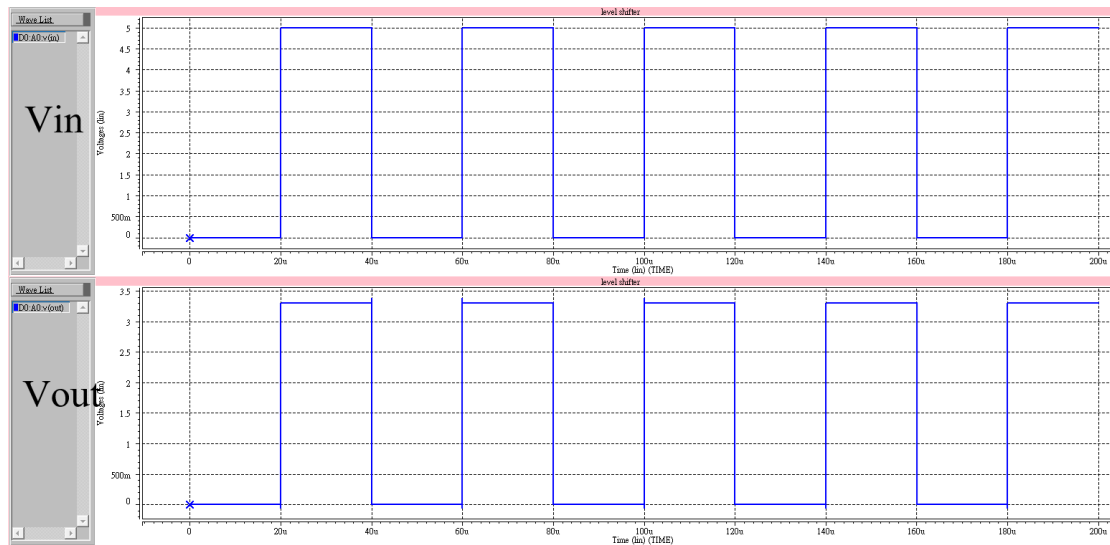


Fig. 41.2-2 The result of Experiment 41.12-1

From 41.1-2, we can see that the height of input pulses decreases from 5V to 3.3V which shows that the circuit works as a decreasing level shifter.